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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/637,145	08/08/2003	Yong Lu	MICRON.229A	3409
20995	7590	02/09/2005	EXAMINER	
KNOBBE MARTENS OLSON & BEAR LLP			LUU, PHO M	
2040 MAIN STREET			ART UNIT	
FOURTEENTH FLOOR			PAPER NUMBER	
IRVINE, CA 92614			2824	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/637,145

Applicant(s)

LU ET AL.

Examiner

Pho M. Luu

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-40 is/are pending in the application.
- 4a) Of the above claim(s) 14-26 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 27-39 is/are allowed.
- 6) ☒ Claim(s) 1-4, 8, 9 and 40 is/are rejected.
- 7) ☒ Claim(s) 5-7 and 10-13 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 11/10/03.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☒ Other: Search History.

DETAILED ACTION

Reply to Election/Restrictions

1. Applicant's election without traverse of Group I, Claims 1-13 and 27-40 filed 15 November 2004 is acknowledged. The changes and remarks disclosed therein were considered.
2. Claims 14-26 have been canceled.
3. Claims 1-13 and 27-40 are pending in the application.

Specification

4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

5. The abstract of the disclosure is objected to because it uses the phrase “**the present invention relates to**” in line 4, which is implied. Correction is required. See MPEP § 608.01(b).

Information Disclosure Statement

6. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 10 November 2003. The information disclosed therein was considered.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1–4, 8-9 and 40 are rejected under 35 U.S.C. 102(e) as being anticipated by Black et al. (US. 6,542,000).

Regarding claims 1-3, Black et al. in Figure 1 discloses a memory device (10) having data line and a giant magneto-resistance GMR (22, 24) storage circuit comprising at least one GMR (22, 24, see column 6, lines 49-51 and also 22, 24 to storing of information inside cell 10, see column 7, lines 57-59) storage cell that is

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coupled to the data line (for example, electrical line 34, 36 such as write data line, column 7, lines 50-51) wherein the GMR storage cell magnetically stores a value indicative of the value of the data line upon receipt of a pre-selected signal (see column 7, lines 50-63) and

a power down detector (the circuit 10 work with power or without power, see column 8, line 20) that detect when power to the memory device is being lost (for example, when power lost, GMR 22, 24 would hold their state via magnetic field which can be used to program or write data in circuit 10, see column 8, lines 22-31) and generates the pre-selected storage signal (34, 36) wherein the power down detector is adapted to provide a pre-selected storage signal that has a sufficient pulse width to change the magnetic state of the GMR storage cell when detecting that the power to the memory device is being lost (see column 8, lines 20-31).

With respected to claim 4, Black et al. in Figure 1-2 further disclosed a memory device (10, Figure 1) wherein the pulse (voltage Vdd) generating circuit includes a logic gate having a first and second input (input 42 in1 coupled to the gate 40A-40B and input 44 in2 coupled to the gate 40C-40D in Figure 2) and a delay circuit (10A-10C, Figure 2) wherein the charge from the charge storage device is simultaneously apply directly to the first input and delay circuit provide an input signal to the second input of the logic gate a pre-selected time period after the application of the charge to the first input of the logic gate.

With respected to claim 8, Black et al. in Figure 1 further disclosed a memory device including an isolation transistor (MP2 12, MN2 14, MP1 16, MN1 18) interposed between the charge storage (22, 24) device and the power supply (Vdd).

With respected to claim 9, Black et al. in Figure 1 further disclosed a memory device including the pulse generating circuit (supply voltage Vdd) that is a rising/failing edge (inverter 12, 14 provided the rising/failing edge coupled to power supply Vdd 28) signal in response to receiving signal from the power supply indicative of the power to the memory device being lost.

9. As per claim 40 of method, they encompass the same scope of invention as to that of claims 1 of apparatus, except they draft in method format instead of apparatus format. The claims are therefore rejected for the same reason as set forth above.

Allowable Subject Matter

10. Claims 5-7 and 10-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 5, the prior art of record do not disclose or suggest a first state to a second state upon receipt of the input signal on the first input and then changes back to the first state form the delay circuit on the second input.

Regarding claim 10, the prior art of record do not disclose or suggest a second layer can be magnetized in either the first fixed direction or a second direction that is opposite the first direction and a spacing layer interposed between the first and second magnetic layer.

Regarding claim 11, the prior art of record do not disclose or suggest a second conductive layer is substantially perpendicular to the first conductive race wherein the intersection point at which the first and second is proximate to at least one GMR cell.

12. Claims 27-39 are allowed.

The following is an examiner's statement of reasons for allowance:

There is no teaching or suggestion in the prior art to: "a load transistor that receives the output pulse signal and generates a pre-selected storage signal that has a sufficient pulse to change the magnetic state of the GMR storage cell when detecting that the power to the electronic device is being lost" as claim in the independent claim 27.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Black et al. (US. 6,317,359) disclosed the device including giant magneto resistive GMR effect storage device as the function data storage unit.

13. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Pho M. Luu whose telephone number is

571.272.1876. The examiner can normally be reached on M-F 8:00AM – 5:00PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Richard Elms, can be reached on 571.272.1869. The official fax number for the organization where this application or proceeding is assigned is 703.872.9306 for all official communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PML
4 February 2004



RICHARD ELMS
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